National Aeronautics and Space Administration

NASA Engineering and Safety Center Technical Bulletin No. 10-01

Power MOSFET Thermal Instability

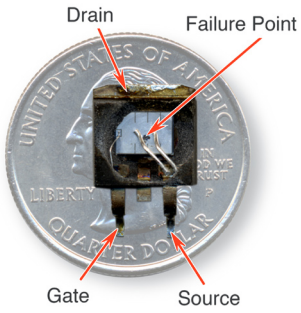
In the quest for faster switching times and lower "on resistance" the Metal-Oxide Semiconductor Field-Effect Transistor (MOSFET), produced since 1998, has achieved most intended goals. Unfortunately, lower "on resistance" and higher switching speeds in the designs now being produced allow the charge carrier dominated region to develop conditions that could lead to thermal runaway. Temperatures above 450º C on any location within the part can cause the metals to begin migrating causing a fatal short circuit.

Applicability

Any power MOSFET that is used with a low gate voltage (not switched mode) for periods of time greater than 10 microseconds. The problem is more pronounced with parts produced since 1998.

Background

Based on recent testing and failure investigations, it appears that the "old" manufacturer application curves are inaccurate with regard to application of some MOSFET parts. These parts may be used extensively in flight hardware and ground support equipment.



Failed Field-Effect Transistor

The push for faster switching and lower "on resistance" power MOSFETs resulted in an unintended consequence similar to the secondary voltage breakdown effect that has not been seen since the prime of the bipolar transistor. When MOSFETs are in the charge carrier dominated region (low gate to source voltage, Vgs) the device allows more current to flow as the temperature increases causing a thermal runaway. It was discovered that the safe operating area (SOA) curves provided by the manufacturers were lacking in describing the region of thermal instability. The problem was identified during a test of a protection circuit that provided a low voltage on the gate of a MOSFET, which failed within seconds. The MOSFET was replaced and a new corrected test was performed. The outcome of the second test was the failure of the second MOSFET. Examination of the de-lidded part revealed a "bulls-eye" heating pattern and aluminum spheres. The failure mode for the two MOSFETs was determined to be common and was the result of the MOSFETs being placed in a thermal runaway condition when the gate voltage was low, but well within the SOA for the MOSFET. This problem, known as "thermal instability" in the industry, has been experienced in the automotive industry since 1997 when advanced, very fast, switching MOSFET devices became available and found wide usage.

MOSFET Failures inside the Advertised SOA

Thermal runaway is a problem affecting a wide range of modern MOSFETs from more than one manufacturer. Older parts can also display thermal runaway, usually well outside the SOA.

Therefore, one may experience other problems first with those older parts. Thermal runaway is caused at low gate to source voltages when the drain current increases at higher temperatures causing a positive feedback effect. Thermal runaway is currently over a larger area of the Vds-Id plane and inside the advertised SOA. The recommended new limit for the SOA can be determined using the Spirito stability formula where Stability (S) is less than one. When S equals one, the calculated temperature approaches an infinite value theoretically. A proper derating is necessary to bring the temperature down to a value below the MOSFET failure temperature. As found in testing, the leakage current of a MOSFET starts to become uncontrollable at about 250º C, so the standard temperature limit of 175º C is recommended. However, the dynamic temperature at the hottest point within the device must be constrained to safe limits.

References

1) IRF510 Data Sheet: 5.6A, 100V, 0.540 Ohm, N-Channel Power MOSFET'; Fairchild Semiconductor; January 2002.

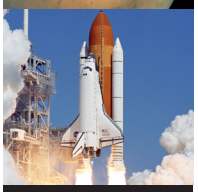
2) Marie Denison, Martin Pfost, Klaus-Willi Pieper, Stefan Märkl, Dieter Metzner, Matthias Stecher; Influence of Inhomogeneous Current Distribution on the Thermal SOA of Integrated DMOS Transistors; Proceedings of 2004 International Symposium on Power Semiconductor Devices & ICs; Kitakyushu; pp. 409–412.

3) P.L.Hower and P.K.Govil; IEEE Transactions on Electron Devices; Volume ED-21, Number 10; October 1974, pp. 617–623.

4) P. Spirito, G. Breglio, V. d'Alessandro, N. Rinaldi; Analytical Model for Thermal Instability Of Low Voltage Power MOS and S.O.A. In Pulse Operation; 14th International Symposium on Power Semiconductor Devices & ICS; Santa Fe, NM; 4–7 June 2002; pp. 269–272.

For information contact the NESC at: www.nesc.nasa.gov



NESC tech bulletin